IN THE SPECIFICATION:

Please amend the following paragraphs as indicated:

[0012] The interface 100 includes a plurality of pins (101). The pin configuration ~~itself~~ in the interface 100 can be any functional configuration and can be used as address/data bus lines between the POD module 102 and the host 104. To provide the DMA function between the POD module 102 and host 104 one of the pins (103) in the interface 100 can act as an interface pin or a DMA pin. Note that some standard interfaces, such as the NRSS-B interface, includes one or more reserved pins that are normally functionally inactive. These reserved pins in the standard established interface 108 can be selectively used by the invention as DMA pins in the configured interface 106 to integrate the POD module 102 and the host 104. Alternatively, the pins can have an established functional pin layout that is selectively changed to a reconfigured functional pin layout to allow DMA transfer and/or shared memory access to occur between the POD module 102 and the host 104. In this case, the pins would have dual functions, with a first function assigned by a standard established functional pin layout acting as the established interface 108 and the second function, such as a DMA transfer function or a shared memory function, provided by a reconfigured functional pin layout acting as the reconfigured interface 106.